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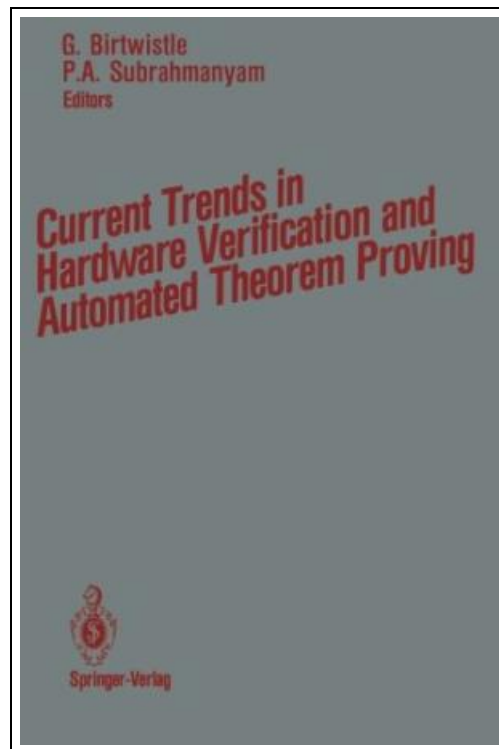G. Birtwistle
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Reviews

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CURRENT TRENDS IN HARDWARE VERIFICATION AND AUTOMATED THEOREM PROVING (PAPERBACK)

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Springer-Verlag New York Inc., United States, 2012. Paperback. Condition: New. Language: English . Brand New Book ***** Print on Demand *****.This report describes the partially completed correctness proof of the Viper block model . Viper [7,8,9,11,23] is a microprocessor designed by W. J. Cullyer, C. Pygott and J. Kershaw at the Royal Signals and Radar Establishment in Malvern, England, (henceforth RSRE) for use in safety-critical applications such as civil aviation and nuclear power plant control. It is currently finding uses in areas such as the de- ployment of weapons from tactical aircraft. To support safety-critical applications, Viper has a particulary simple design about which it is relatively easy to reason using current techniques and models. The designers, who deserve much credit for the promotion of formal methods, intended from the start that Viper be formally verified. Their idea was to model Viper in a sequence of decreasingly abstract levels, each of which concentrated on some aspect ofthe design, such as the flow ofcontrol, the processingofinstructions, and so on. That is, each model would be a specification of the next (less abstract) model, and an implementation of the previous model (if any). The verification effort would then be simplified by being structured according to the sequence of abstraction levels. These models (or levels) of description were characterized by the design team. The first two levels, and part of the third, were written by them in a logical language amenable to reasoning and proof. Softcover reprint of the original 1st ed. 1989.

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