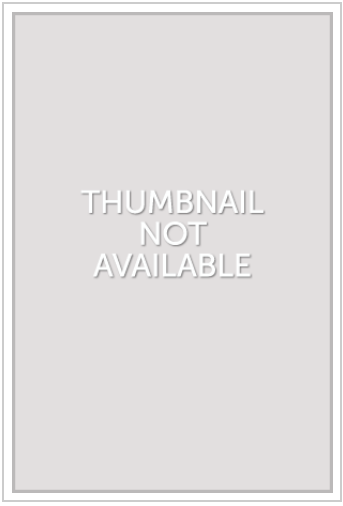

VHDL: Design, Synthesis and Simulation

By Debaprasad Das

OUP India, 2018. Soft cover. Condition: New. 1st Edition. Contents: 1. Introduction to digital logic design. 2. Introduction to VHDL. 3. Dataflow modeling. 4. Behavioral modeling. 5. Structural modeling. 6. Mixed modeling. 7. Concurrent statements. 8. Sequential statements. 9. Advanced VHDL. 10. Arithmetic logic unit design. 11. Model simulation. 12. Delay modeling. 13. Verification and testing. 14. Synthesis. 15. Place and route. 16. File I/O. 17. Floating-point arithmetic. 18. Design with FPGA and CPLD. 19. Memories and buses. 20. Design examples. 21. Introduction to verilog. VHDL: Design, Synthesis, and Simulation is a textbook designed to meet the requirements of undergraduate students of electrical engineering (EE), computer science and engineering (CSE), information technology (IT), and electronics and communication engineering (ECE). This book would be useful for postgraduate students studying the related course while it would also serve as an invaluable reference for practising engineers. The book begins with an introduction to the concepts of digital logic design and moves on to cover the fundamentals of VHDL. Modelling types such as dataflow, behavioural, structural and mixed modelling are covered as separate chapters. Chapters on concurrent statements and sequential statements are covered next. The design aspect of the subject begins with the chapter...

Reviews

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