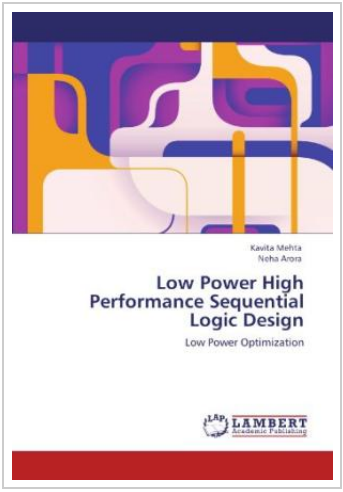

Low Power High Performance Sequential Logic Design

By Kavita Mehta

LAP Lambert Academic Publishing Jun 2012, 2012. Taschenbuch. Condition: Neu. Neuware - Latches and flip-flops have a direct impact on power consumption and speed of VLSI systems. Therefore study on low-power and high performance latches and flip-flops is inevitable. In this book we delve into the details of TSPC pulsed latch design and optimization for low power. The proposed circuit uses MTCMOS technique resulting in significant energy savings. This proposed circuit outcomes existing designs and shows the best result. The leakage power is reduced by using best technique among all run time techniques viz. MTCMOS. Thereby comparison of different conventional flip-flops and TSPC flip-flop in terms of power consumption, propagation delays and product of power consumption and propagation delay with SPICE simulation results is calculated. This book also enumerates low power, high-speed design of D flip-flop. It presents technique to minimize subthreshold leakage power as well as the power consumption of the CMOS circuits. The proposed circuit in this book shows a design for D flip flop to increase the overall speed of the system as compared to other circuits. This technique allows circuit to achieve lowest power consumption 96 pp. Englisch.

Reviews

Extremely helpful to any or all category of individuals. It really is rally fascinating throgh studying time period. I am just quickly could possibly get a pleasure of reading a composed ebook.

-- ***Lawrence Keeling***

This publication may be worthy of a read through, and a lot better than other. It is among the most incredible book we have read through. Your daily life period will be change when you total reading this article publication.

-- ***Garett Baumbach***